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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
00100.00.0130	

I hereby certify that this correspondence is being forwarded via electronic submission to: Electronic Business Center, Commissioner for Patents, Mail Stop AF	Application Number	Filed
on May 21, 2008	10/074,064	February 12, 2002
Signature Christine Wright	First Named Inventor: Antonio Asaro et al.	
Typed or printed name Christine A. Wright	Art Unit: 2111	Examiner: Paul R. Myers

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 34,414
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature

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Telephone number

May 21, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Antonio Asaro et al.	Examiner:	Paul R. Myers
Serial No.:	10/074,064	Art Unit:	2111
Filing Date:	February 12, 2002	Docket No.:	00100.00.0130
Confirmation No.:	6702		

Title: **METHOD AND APPARATUS FOR A DATA BRIDGE IN A COMPUTER SYSTEM**

Mail Stop AF
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Applicants respectfully submit that the Examiner's rejections include clear errors because the Examiner failed to address claim language and the references do not teach what the Examiner alleges.

Claims 1, 4-9, 19, 22-23 and 25-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gillespie in view of Surugucchi and Venkat. Claims 2-3, 20-21, 24 and 33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gillespie in view of Surugucchi and Venkat as applied to claim 1 and further in view of Applicants' admitted prior art.

As to claims 1, 8 and 28, The Advisory Action sums up the Examiner's position by stating that Applicants' arguments are not persuasive since "populating with data is configuring." (Advisory Action, page 2). However, Applicants respectfully submit that there is a difference between populating a register with values and configuring a register to make it a read or writable register. Applicants respectfully submit that the claims themselves require something very different than simply populating a register with data. For example, claim 28 requires memory that contains both initial values and mask values for use in forming a register and in addition, a configurable register that includes register configuration logic and at least one register flop to contain an initial value and at least one mask flop that generates a mask that for the configuration logic and wherein the register configuration logic configures the at least one register flop to be read and/or writable based on the at least one mask value stored in the memory. As such, the configuration described in the claim refers to configuring a register to be read and/or writable – not populating the register with a value. As such, the Examiner's reasoning is clear error.

The Office Action admits that the Gillespie reference does not teach that a data bridge read only memory stores at least initial values and mask values for each ASIC of a plurality of ASICs. Applicants also respectfully submit that the Office Action appears to mischaracterize Gillespie for failing to teach other subject matter. For example, the Office Action alleges that as to Gillespie, the base address registers "would inherently need to be configured." Applicants respectfully submit that what Gillespie would actually inherently need is that base address registers be populated with data values. Gillespie would not need to have any base address registers "configured" as claimed, for example, to be configured to be read or writable based on read/write mask values that are stored in read only memory. In their response to final action, Applicants respectfully requested a showing as to where such inherency is taught or why the configuration as to readability or writability of the base address registers would be required in Gillespie. As known in the art, the base address registers merely contain data identifying the base address register. There is no need for mask values that configure registers to be read and or writable. Applicants request for a showing was not addressed. This was clear error.

Also the Applicants respectfully submitted that the Surugucchi reference appears to have been misapprehended. Surugucchi is directed to a different system from that taught by Gillespie or Applicants' claimed invention. In fact, there is no read only memory used in Surugucchi and Surugucchi utilizes separate bridge circuitry and separate BASS circuit in order to simply populate configuration registers. The use of the word "mask register" as specifically described in Surugucchi is a register, not RAM, and also merely stores contents which are values—not mask values—that set the memory base address register to contain initial address location information. The mask values in Surugucchi have nothing to do with creating a register to be writable or readable.

As stated in Surugucchi, the bridge assist device (BASS) is an exposed PSI device that is used to acquire the system memory address space required by interface controllers. The memory address space is then partitioned by a controller and assigned to each of the hidden PCI devices. The BASS appears to the host system as a device with a memory space requirement which is the sum total of the space needed by the interface controllers. In realty, the BASS is a dummy device and does not use disk space. (Column 2, lines 52-60).

The BASS uses two configuration register spaces 258 and 260. As specifically stated in column 10 of Surugucchi in reference to the word "memory mask register," the contents of this register are used to set the memory base address register contents which are initial values and not

mask values that change a base address register to be read or writable. As specifically stated in column 10:

> "The first configuration register space 258. This memory space is used by the interface controllers 218 to communicate with the local CPU 214. The base address of the memory space is set in the PCI memory base address register (offset 10h) and the first configuration register space 248 (see Fig. 10). The BASS control logic unit 254 then updates the corresponding register (i.e., PSI memory base address register, offset 10h). In the second configuration space 260 with the same value . . . (column 10, lines 5-13).

As such, Surugucchi uses the word mask to refer to actual initial values or contents of a register as opposed whether the register is a read or writable register. As such, Applicants respectfully submit that the Surugucchi reference teaches a known prior art systems that 1 – does not include a ROM in any data bridge and 2 – merely use the contents of one register to be written as the contents of a base address register.

In addition, the Office Action alleges that the corresponding bridge in Surugucchi is 210 and 212 alone or 212 taken together with 210. Again, Applicants respectfully note that the bridge 210 is not a bridge to a whole system but is a bridge to a local CPU and that the configuration register space of the local PCI bridge contents thereof, such as the base address register, is populated by the BASS 212. Again, which is not ROM and which only includes initial values for the registers in the local to PCI bridge.

As such, since the configuration space in Surugucchi is used to "write data into the first configuration register space and to read from the first configuration register space" (column 3, lines 11-16) and since Surugucchi describes the "mask register" as actually containing data which serves as the contents of the base address register, and hence initial values of the base address register of the local bridge, substituting this teaching in Gillespie would merely result in the ROM of Gillespie storing initial base address register values.

As used in the claims, Applicants distinguish between "initial values" and "make values" in the read only memory. They are different information used for different purposes and control the registers in a different manner since the initial values are the contents stored in the registers and the mask values configure the registers to be, for example, read and/or writable. No such teaching or disclosure is set forth in either Gillespie or Surugucchi and in fact Surugucchi in terms of base address register population, teaches no more than what Gillespie and Gillespie admittedly does not teach the claimed subject matter.

Since the references do not teach what is alleged, Applicants respectfully submit that the claims are in condition for allowance.

Claims 10-11, 13, 15-17 and 34-35 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gillespie in view of Surugucchi and Venkat as applied to claim 1 and further in view of Prabhu. Claim 34 further requires the data bridge system of claim 1 wherein the configurable register includes register configuration logic and at least one register flop to contain an initial value in at least one mask flop that generates a mask bit for the configuration logic and wherein the register configuration logic configures the at least one register flop to be read and/or writable based on at least one mask value stored in the memory. None of the references teach a configurable register.

As to the Prabhu reference and claims 34 and 35, Applicants respectfully submit that these claims are different from claim 28 in that the claims require a data bridge system as claimed in independent claims and such language cannot be disregarded. Furthermore, as to claim 28, in the "response arguments" section, the Examiner states that "While the Examiner does not agree with the Applicant's assessment that Prabhu's configuring a register only by the manufacturer 'preconfigured' is configured." Applicants respectfully challenge such an assertion since the claim specifically requires "at least one configurable register." It does not claim a configured register. As such, the register as claimed has not yet been configured but the initial value and the mask value are used to configure the register flop to be read and/or writable based on at least one mask value stored in the memory. Again, there is no "memory" in Prabhu nor is there any such memory in Gillespie, Surugucchi or Venkat, nor is there any suggestion to have such a memory. In addition, Applicants respectfully submit that there is a difference between a configurable register and one that already has been configured. Applicants also respectfully note that the Examiner admits that none of the references teach a "mask bit" pursuant to the statements on the top of page 4 in the Office Action. It also appears that the statement indicating that "initial data" is stored in read only memory is not accurate since the cited references as noted above do not teach such structure and the "mask bit" as claimed is also not taught in any of the references and the requisite combination on any suitable way to suggest the claimed subject matter.

As to claims 34 and 35 for example, which is required to be part of a data bridge system, Applicants respectfully note that Applicants' claimed invention offers advantages over known systems, even assuming for argument's sake that write protect bits have been used in some other

art other than data bridge systems for example. However, assuming masked bits are known in some art for some time, Applicants respectfully submit that to date Applicants are unaware of the claimed invention that shows a long felt and unmet need. No data bridge is known or suggested in the art that is coupled to a plurality of ASICs for example, wherein the data bridge has a read only memory that stores initial values and mask values for each ASIC of the plurality of ASICs. The Surugucchi and Gillespie reference dealing with the bridge circuits are similar to those described in Applicants' Background of the Invention section and suffer from the same problems. Applicants appreciate the Examiner's thoughts but respectfully request reconsideration in view of the above remarks.

Claim 28 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,675,292 (Prabhu). Applicants respectfully reassert the relevant remarks made above with respect to Prabhu and as such, this claim is in condition for allowance.

Claims 14 and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gillespie in view of Surugucchi, Venkat and Prabhu as applied to claim 10 and further in view of Applicants' admitted prior art. These claims are allowable at least as depending on an allowable base claim.

Withdrawal of the rejections of the claims is respectfully requested and a Notice of Allowance is respectfully requested.

Respectfully submitted,

Date: May 21, 2008

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